Attorney Docket No.: FIS920030352US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re PATENT APPLICATION Of:	
Tien-Jen Cheng et al.	
Appln. No.: 10/707,892	Art Unit: 2815
Filed: January 21, 2004	Examiner: M. C. Landau
For: DEVICE WITH PROBABLE AREA ARRAY PADS	

DECLARATION UNDER 37 C.F.R. §1.131

Mail Stop **AMENDMENT**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We, Tien-Jen Cheng, David E. Eichstadt, Jonathan H. Griffith, Sarah H. Knickerbocker, Samuel R. McKnight, Kamalesh K Srivastava, Kevin S. Petrarca, and Roger A. Quon, inventors for the invention claimed in the above referenced patent application, declare as follows:

Sometime prior to September 18, 2003, we conceived area array pads (hereinafter "Pads") that, when included on a device, such as a semiconductor device and/or structure, may be used for test probing the device;

Attached hereto and marked Exhibit A, is a copy of a presentation explaining our Pads, formation of the Pads, and test results of the Pads, all dates having been redacted therefrom, providing evidence of conception and reduction to practice;

As evidenced in pages 3 and 4 – 6 of Exhibit A, our Pads included:

a terminal metal layer disposed on a passivating layer;

a diffusion barrier layer on said terminal metal layer;

a conducting layer pad on said diffusion barrier;

a hard test barrier layer on, and enclosing (see page 6 of Exhibit A), said conducting layer pad, wherein said hard test barrier layer extends along the sides of said conducting layer pad and said conducting layer pad is completely enclosed by said diffusion barrier layer and said hard test barrier layer; and

a plate passivating layer on said hard test barrier layer;

Sometime prior to September 18, 2003, we reduced our invention to practice as evidenced in pages 8 – 10 of Exhibit A;

All acts, including conception and reduction to practice, occurred in the United States;

We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and

We further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor: Tien-Jen Cheng

Signature: Tien Jen Cheng Date: 10/26/2007

Residence: 75 Hickory Lane, Bedford, New York 10506
Citizenship: US

Post Office Address: Same as Residence

Inventor: David E. Eichstadt

Signature: _____ Date: _____

Residence: 344 Graceland Ave, Des Plaines, Illinois, 60016
Citizenship: USA

Post Office Address: Same as residence

Inventor: Jonathan H. Griffith

Signature: Jonathan H Griffith Date: 10/24/2007

Residence: 8 Budd Lane, Lagrangeville, New York 12540
Citizenship: USA

Post Office Address: Same as residence.

Inventor: Sarah H. Knickerbocker

Signature: Sarah H. Knickerbocker Date: 10/26/07

Residence: 208 Creamery Rd., Hopewell Junction, New York 12533
Citizenship: USA

Post Office Address: Same as residence.

Inventor: Samuel R. McKnight

Signature: _____ Date: _____

Residence: 112 Bruynswick Rd., New Paltz, New York, 12561
Citizenship: USA

Post Office Address: Same as residence

Inventor: Kevin S. Petrarca

Signature: _____ Date: _____

Residence: 28 Laurie Lane, Newburgh, New York, 12550
Citizenship: USA

Post Office Address: Same as residence

Inventor: Kamalesh K Srivastava

Signature: Kamalesh K. Srivastava Date: 10.26.07

Residence: 319 Sheafe Rd., Wappingers Falls, New York 12590
Citizenship: USA

Post Office Address: Same as residence

Inventor: Roger A. Quon

Signature: _____ Date: _____

Residence: 15 Rockefeller Lane, Rhinebeck, New York 12572
Citizenship: US

Post Office Address: Same as Residence

Detailed Embodiment

IBM technology

Microelectronics Division

Disclosure F[redacted]067

EXHIBIT A

Problem Statement:

No Technology or Method exists for testing device performance on area-array, non-compliant metallurgies.

- Testing device performance directly on C4s is common practice, but is destructive
- Testing device performance on FBEOL via metallurgies is possible, but is also disruptive to bumping processes

Proposal

A Means and Method for testing device performance on non-compliant metallurgies which also serve as a C4 ball-limiting metallurgy for bumping after test.

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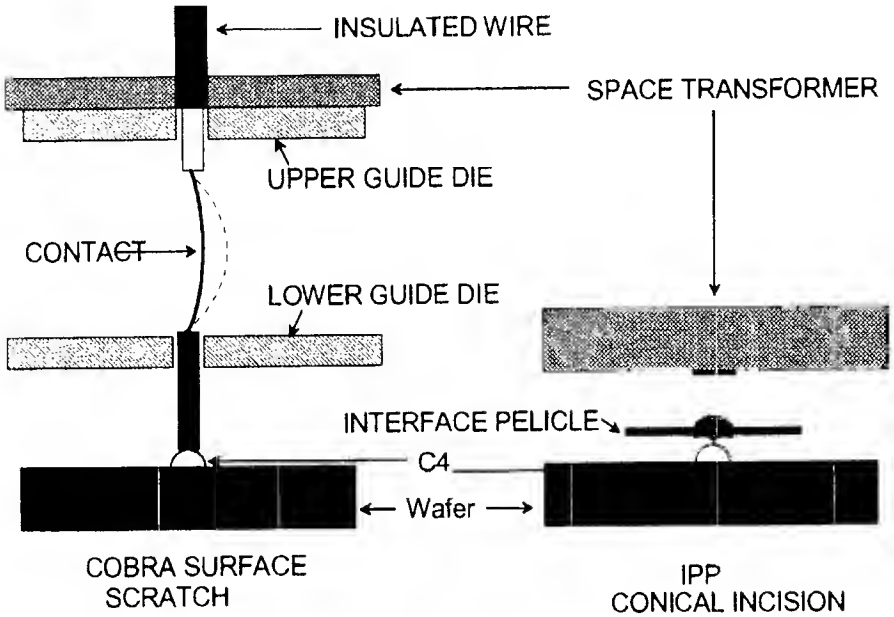
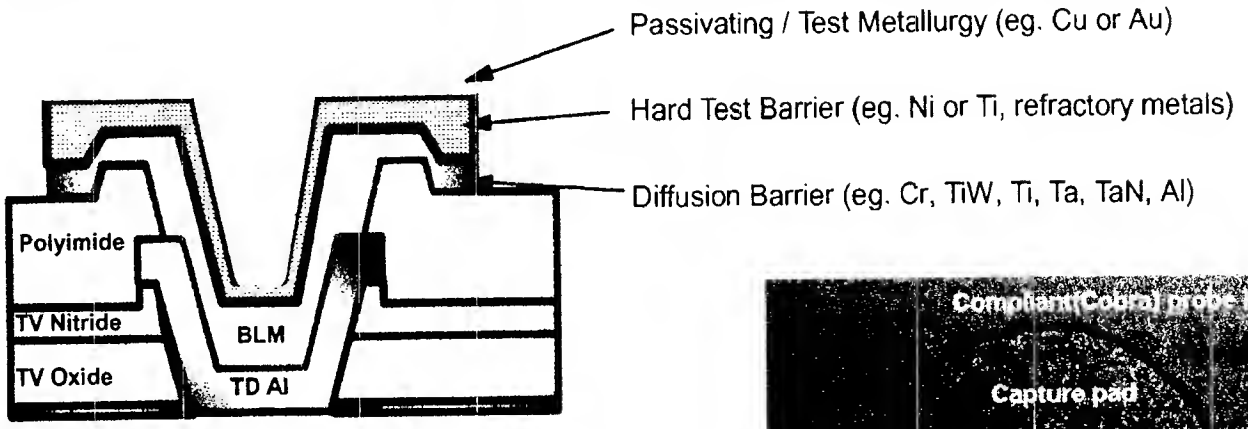
Standard Test Methods ⇨⇨⇨ Deform C4s

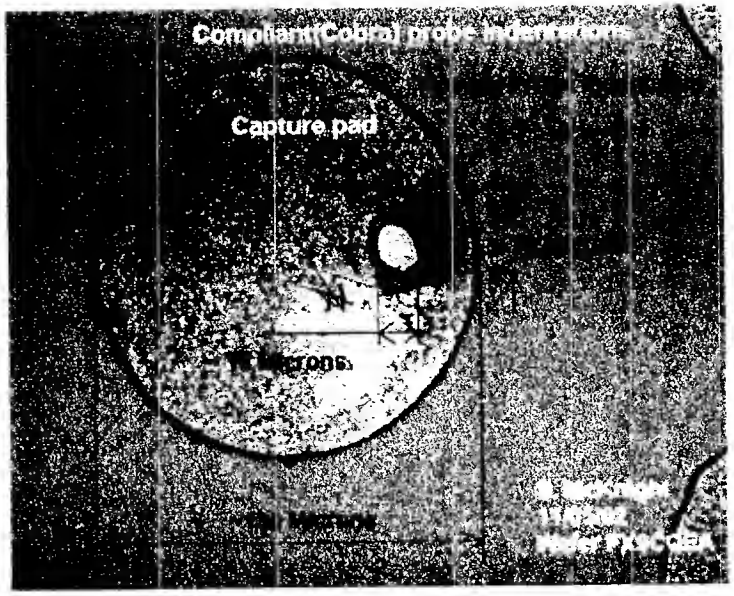


Cobra probe mark on PB free C4

TFI probe mark on PbSn C4

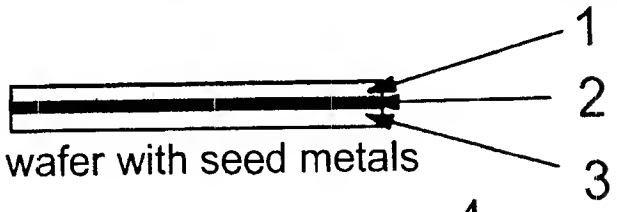
essential elements of a bump metallurgy for test

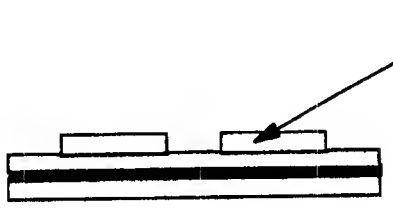


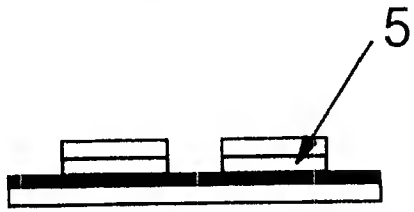


bump metallurgy tested!

Process Flow: Preferred Embodiment

1. 

2. 

3. 

structures

1. seed metals commonly terminating in copper
2. barrier and/or adhesion metallurgy
   e.g. TiW, Ti, Ta, TaN, and so on.
3. substrate
4. patterned resist selectively blocking seed metal
5. copper pad

Process Flow:

4. 

mask remove

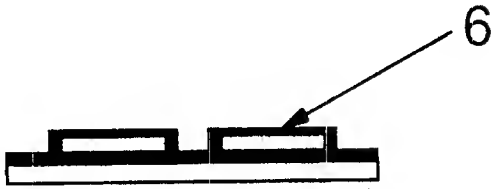
5. 

plate hard test barrier

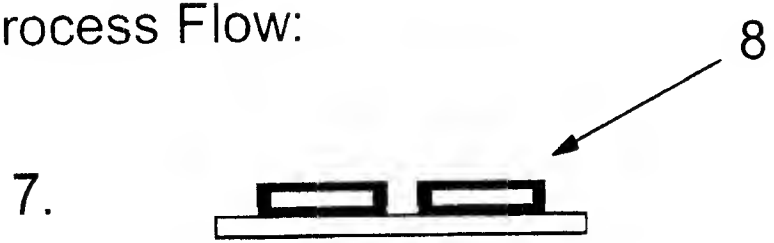
6. 

Plate passivation

structures

2. adhesion/barrier metallurgy serves as plating conducting layer
6. Plate hard test barrier metallurgy (eg. Ni) o' exposed copper seed.
7. application of nickel barrier metallurgy, or other similar metal on which solder can be plated

Process Flow:



structures

8. Sub-etch the diffusion barrier to form the final test metallurgy.

While this method of constructing the test metallurgy is preferred, those skilled in the art could clearly construct the test structure by other means, including, but not limited to thru-hole plating and metal evaporation. These techniques are also encompassed in the spirit of this embodiment.

Invention and Advantages:

Enables MD Foundry

- Capability for wafer-level test prior to bumping offers customers more options for bumping and assembly
- Area-Array Testing on C4 UBM allow MD to track and optimize yields for Foundry Customers

Enhances Test Capability

- Improved signals for measurements as contact resistance between probe and non-compliant metallurgy is LOWER than typical.
- Less force required to make good electrical contact ENABLES Multi-Die Testing from a force perspective
- Less clean and prep work required REDUCES test cycles.

Enable Test Ability for Fine Pitch Designs

- Testing on Pads precludes Deformation and Bulging of solder

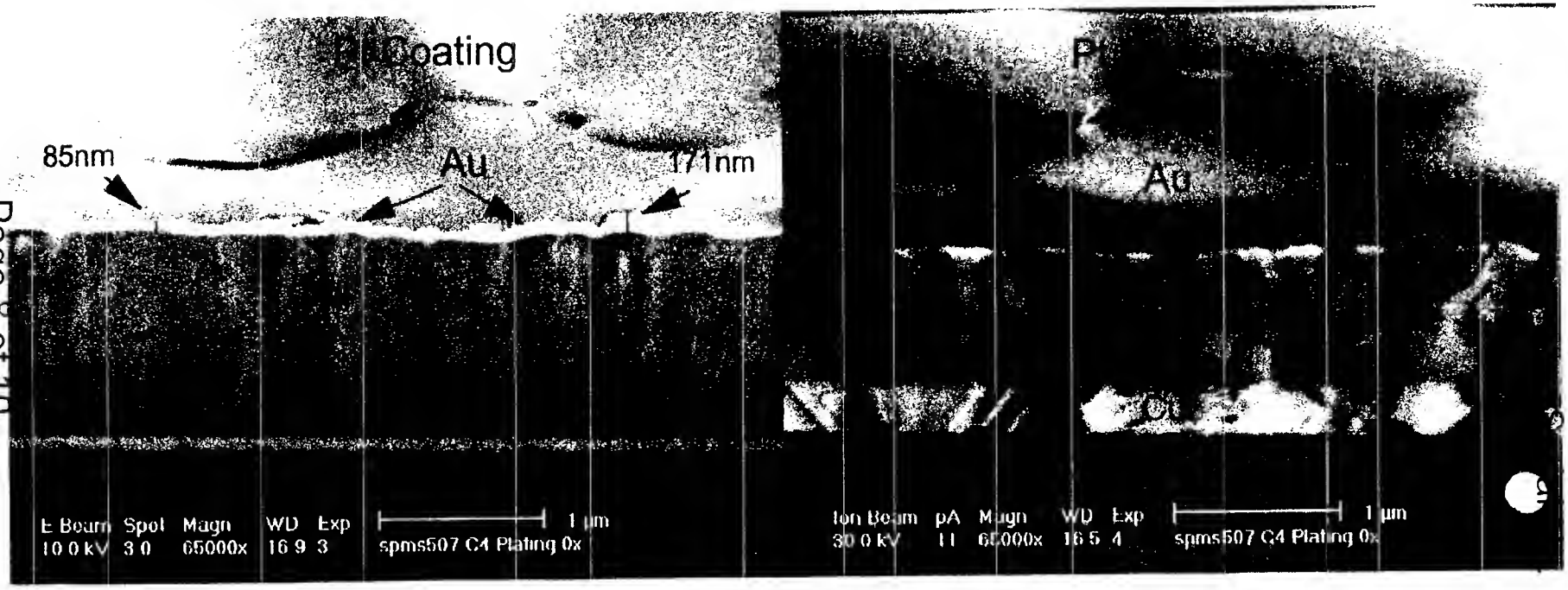
ASG

FIB Analysis

C4 Plating BLM Layer Measurements

Electron Image

Ion Image



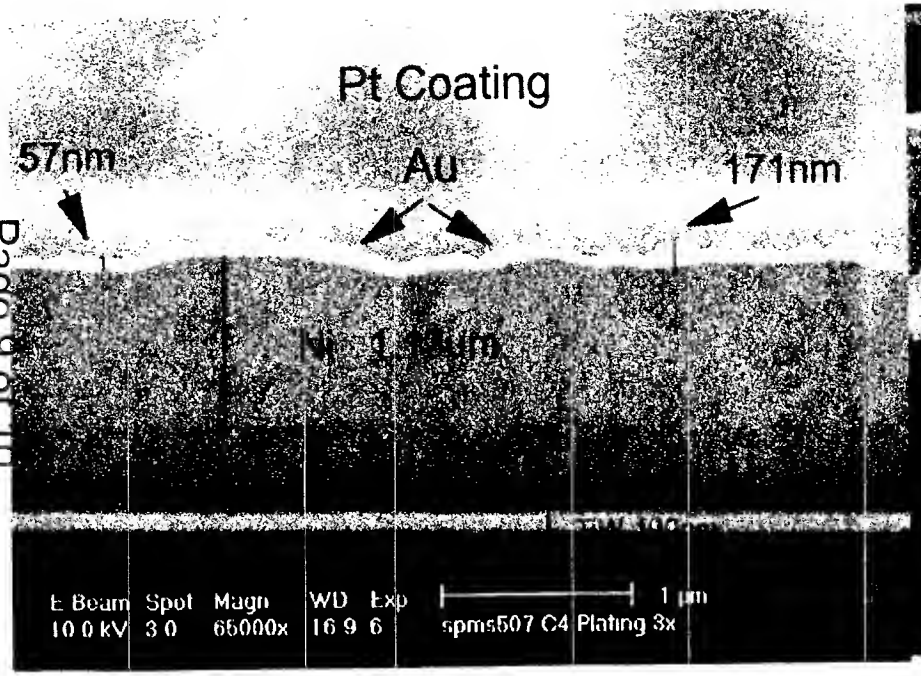
0x REFLOWS

ASG

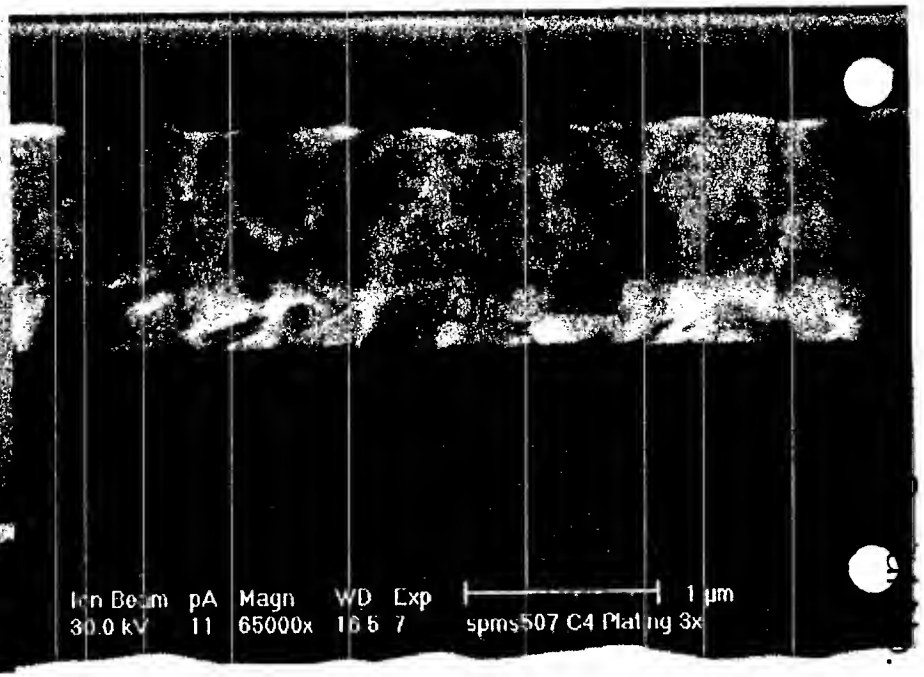
FIB Analysis

C4 Plating BLM Layer Measurements

Electron Image



Ion Image



3x REFLOWS

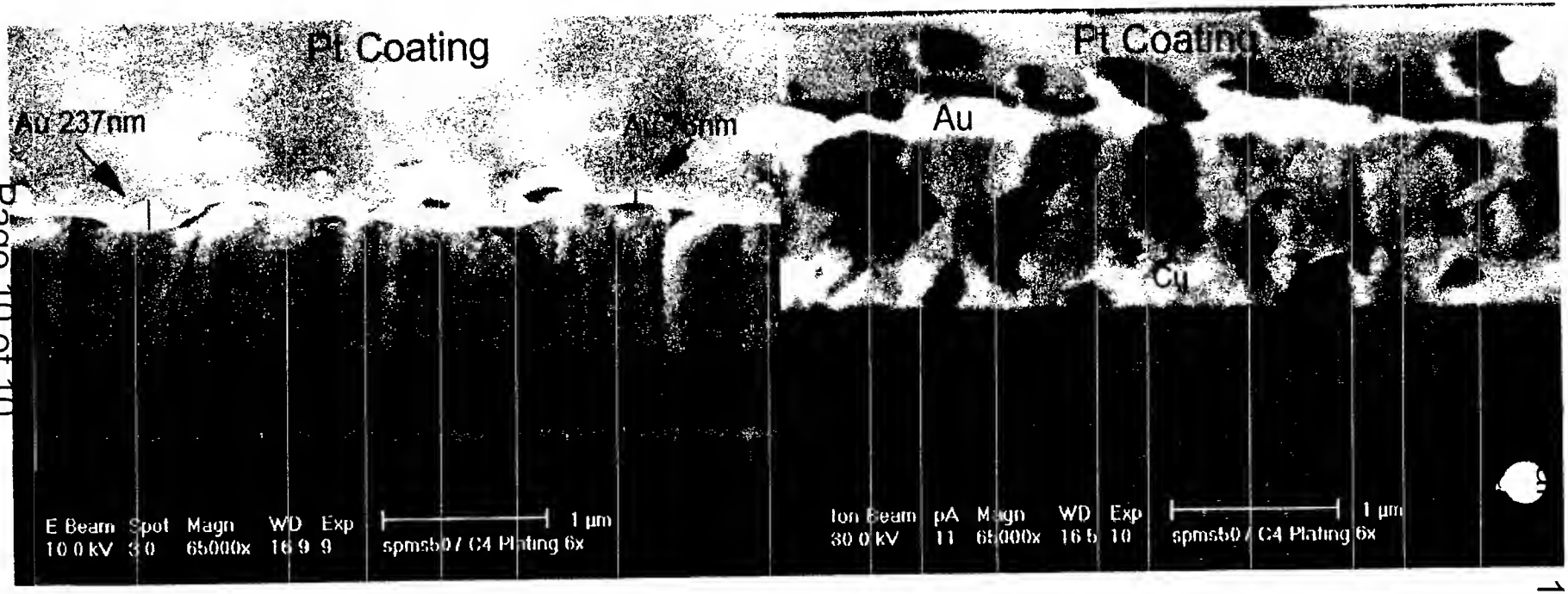
ASG

FIB Analysis

C4 Plating BLM Layer Measurements

Electron Image

Ion Image



6x REFLOWS

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Signature: _____ Date: _____

Residence: 112 Bruynswick Rd., New Paltz, New York, 12561
Citizenship: USA

Post Office Address: Same as residence

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